

REMARKS

Claims 1-12 have been cancelled without prejudice. Claims 13-22 have been newly added. As a result, claims 13-22 remain pending in the present application. Reconsideration of the application in view of the foregoing amendments and following comments is respectfully requested.

Claim Rejection - 35 U.S.C. §102

With respect to Paragraphs 1 and 2 of the outstanding Office Action, the Examiner rejected claims 1-12 under 35 U.S.C. §102(b) as being anticipated by Tomes et al (U.S. 5,278,086). Claims 1-12 have been cancelled without prejudice, and claims 13-22 have been newly added. Of the newly added claims, only claims 13 and 18 are independent.

Accordingly, applicants respectfully request that the rejection be withdrawn.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). **"The identical invention must be shown in as complete detail as is contained in the ... claim."** *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). **The elements must be arranged as required by the claim**, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). (MPEP §2131)

With particular reference to Tomes, the purpose of the prior art reference is to provide a gate resistor for preventing short-circuiting of the address lines in the event of a gate short-circuit occurring in any of the transistors (in abstract), Tomes failed to teach the same gate voltage deformation means as the claimed invention.

In Tomes, the gate of each TFT connects to the respective address line via a gate resistor 33, 35, 37, 39 in Fig. 2. That is, the gate resistor is between the address line 25 and the gate of each TFT. Hence, these gate resistors have effects only on the directly connected TFT, not a series of TFTs connected to the same scan line. These gate resistors will act to prevent the address line from also becoming short-circuited (column 3, lines 29-34). Therefore, these gate resistors have nothing related to deformation of the gate voltage input from the input terminal of the corresponding scan line. Furthermore, the drain of each TFT (T11, T12, T21, T22) connects only to the LC cell (C11, C12, C21, C22) in Fig. 2.

However, in independent claim 13 of the present application, the gate deformation means located on the scan line and **only** between the gate of the first pixel TFT and an input terminal of the scan line. The gate voltage deformation means is used to deform the input gate voltage waveform and defined by using means-plus-function language. In independent claim 18, the gate deformation means is also located on the scan line and between the gate of the first pixel TFT and an input terminal of the scan line. The gate deformation means is used to generate a deformed gate voltage, which is transmitted to every pixel TFT connected to the same scan line. Hence, the gate input voltage waveform of each pixel TFT connected to the same scan line is deformed.

MPEP §2182 (Scope of the Search and Identification of the Prior Art) states that the application of a prior art reference to a means or step plus function limitation requires that the prior art element perform the identical function specified in the claim. Accordingly, since Tomes's gate resistors do not perform the same function as specified for the gate voltage deformation means in claims 13 and 18 of the present application, claims 13 and 18 are novel over Tomes.

Moreover, Tomes's gate resistors are respectively located between the address line and the gate of each TFT, as shown in Fig. 2. Hence, even if Tomes's gate resistors performed the identical function as the gate voltage deformation means in claims 13 and 18, it would still be different from the gate voltage deformation means located on the scan line and between the gate of the first pixel TFT and an input terminal of the scan line, as defined in claims 13 and 18.

Furthermore, the drain of each TFT connects to a LC cell only in Fig. 2 of Tomes. However, the drain of each pixel TFT connects to a liquid crystal capacitor and a storage capacitor in claims 13 and 18 of the present application.

Accordingly, Applicant respectfully submits that independent claims 13 and 18 are allowable over the art of record and respectfully requests the 35 U.S.C. §102(b) rejection to be reconsidered and withdrawn. In addition, insofar claims 14-17 and 19-22 respectively depend from independent claims 13 and 18 and add further limitations thereto, these claims should be also allowable over Tomes.

Reconsideration and withdrawal of this rejection is respectfully requested.

Conclusions

For all of the above reasons, applicants submit that the specification and claims are now in proper form, and that the claims define patentably over prior arts. Therefore applicants respectfully request issuance for this case at the Examiner's earliest convenience.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN & BERNER, LLP



Benjamin J. Hauptman
Registration No. 29,310

Customer Number: 22429
1700 Diagonal Road, Suite 300
Alexandria, Virginia 22314
(703) 684-1111
(703) 518-5499 Facsimile
Date: June 27, 2006
BJH/cjf